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Direction and Opportunities

in Heterogeneous Integration using Advanced Packaging

Date: 16 October 2020 (Friday)
Time: 09.30 AM – 11.30 AM (GMT +8)
Platform: CISCO Webex
Registration: https://bit.ly/3czWNIE

E-Certificates will be provided to participants

DR RAVI MAHAJAN
Fellow & Director
Technology & Manufacturing Group
Intel Corporation

Organized by:

IEEE MALAYSIA SECTION
IEEE ELECTRONICS PACKAGING SOCIETY MALAYSIA CHAPTER
IEEE UNIMAP STUDENT BRANCH
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Agenda:

0930 – 0940	Welcoming Remarks
0940 – 1100	Industrial Talk by Dr Ravi Mahajan
1100 – 1130	Q & A

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In recent years, microelectronics packaging, used for Heterogeneous Integration, has become an increasingly important performance enabler. The Heterogeneous Integration Roadmap (HIR), collaboratively driven by IEEE, SEMI and ASME plays an important role in bringing together experts across multiple disciplines and market segments, to develop a broad roadmap. This talk will describe the HIR effort broadly and then focus on one element of the roadmap i.e. Advanced Packaging. Advanced packaging technologies are critical enablers of Heterogeneous Integration (HI) because of their importance as compact, power efficient platforms. In this talk different packaging architectures will be compared primarily on the basis of their physical interconnect capabilities. Key features in leading edge 2D and 3D technologies, such as EMIB, Silicon Interposer, Foveros and Co-EMIB will be described and a roadmap for their evolution will be presented. Challenges and opportunities in developing robust advanced package architectures will be discussed. The talk will conclude with a discussion of overall opportunities in driving the roadmap forward.

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Dr Ravi Mahajan

Director, Technology and Manufacturing Group

Intel Corporation

Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives. He has led Pathfinding efforts to define Package Architectures, Technologies and Assembly Processes for multiple Intel silicon nodes including 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Ravi joined Intel in 1992 after earning Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights have led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques for thermo-mechanical stress model validation.

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His contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award For Excellence and the 2020 ASME EPPD Excellence in Mechanics Award. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE.

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